20.2 An IEEE 802.11a/b/g SoC for Embedded WLAN Applications

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The growing market for wireless voice-over-IP, network gaming, and mobile internet access has fueled the demand for compact, low-power, low-cost WLAN solutions suitable for battery-operated handheld devices. Spectral crowding at 2.4GHz and the abundance of unlicensed bandwidth at 5GHz has resulted in greater demand for dual-band WLAN products that support all three IEEE 802.11a/b/g modes. In this paper, the implementation of a 0.18µm CMOS dual-band IEEE 802.11a/b/g WLAN SoC designed for low-power embedded applications is presented. As shown in Fig. 20.2.1, the SoC is comprised of a dual-band 5GHz/2.4GHz RF transceiver, data converters, baseband PLL, digital PHY, MAC, power management, CPU, and host interface. The SoC supports multiple crystal frequencies to allow sharing of clock resources with its host system.

Figure 20.2.2 shows a block diagram of the RF transceiver. Both the 5GHz and 2.4GHz transmit and receive paths employ a sliding-IF dual-conversion architecture in which the RF local oscillator (LO_{RF}) and IF local oscillator (LO_{IF}) frequencies are at 2/3 f_{RF} and 1/3 f_{RF}, respectively [1, 2]. The LO signals are generated from a fractional-N frequency synthesizer with a tuning range from 3.08 to 4GHz. In 2.4GHz mode, the synthesizer output is divided by two to generate LO_{RF2} (1.6GHz). In 5GHz mode, the synthesizer output provides LO_{RF5} (3.6GHz) directly. An AGC loop is used in the LO_{RF5} buffer to minimize power consumption. Local, resistively-loaded divide-by-two circuits in the transmit and receive blocks are used to generate the quadrature LO_{IF} phases from LO_{RF}.

As shown in Fig. 20.2.3, the fractional-N frequency synthesizer consists of a PFD, a charge pump (CP), integrated loop filter, VCO, 8/9 prescaler, pulse (P) and swallow (S) counters, 3rd-order ΔΣ modulator, and control logic. Separate on-chip voltage regulators power the CP and VCO to reduce supply noise coupling. For some crystal frequencies, the optional reference divider may be used for integer-N frequency synthesis. In fractional-N frequency synthesis, a high reference frequency is desirable so that ΔΣ quantization noise is generated at frequencies well above the synthesizer loop bandwidth. A passive 3rd-order loop filter is used to attenuate out-of-band ΔΣ quantization noise that appears in the CP output. The 3rd pole of the filter must be sufficiently greater than the loop bandwidth to avoid instability.

The wide synthesizer tuning range needed to cover the entire 5GHz and 2.4GHz bands is achieved using a varactor-tuned LC-tank VCO that incorporates an 8b resolution switched-capacitor bank for coarse frequency tuning. Upon startup or RF channel change, the control logic performs a binary search for the correct VCO capacitor settings. A fast lock time of 80µs is achieved using a closed-loop search algorithm in which the VCO control voltage (V_C) is forced to mid-rail and the P and S counters are reset at the start of each step to align the phase of the reference and feedback clocks. One drawback of capacitively tuned LC-tank VCOs is the large variation in voltage-to-frequency gain with oscillation frequency. Control logic varies the CP current with VCO frequency to compensate for systematic variations in its gain. With a 19.2MHz crystal, the synthesizer phase noise measured at the 5GHz and 2.4GHz transmitter outputs, is -93dBc/Hz and -99dBc/Hz, respectively, at a 100kHz offset.

As shown in Fig. 20.2.2, the 5GHz and 2.4GHz receive signal paths share the same analog baseband circuits. The current-mode I and Q outputs of the IF mixers are low-pass filtered by two programmable-gain 4th-order Butterworth g_m-C filters and digitized at 40/44 MS/s by a two-input, time-multiplexed, 9b pipelined ADC. The time-multiplexed ADC running at twice the sampling rate is almost half the size of a dual pipelined ADC implementation. Shown in Fig. 20.2.4, the ADC input S/H circuit simultaneously samples both I and Q inputs and time-multiplexes the I and Q signals that are quantized by subsequent stages of the ADC. The measured NF of the receive chain is 5.5dB at 5GHz and 5.0dB at 2.4GHz. The overall 5GHz and 2.4GHz receiver sensitivity is -91dBm and -94dBm, respectively, for a data rate of 6Mb/s, and -73dBm and -76dBm for a rate of 54Mb/s.

The 5GHz and 2.4 GHz RF transmit paths also share analog baseband circuits. Two 11b, 176MS/s current-steering DACs convert the digital baseband I and Q signals into a pair of differential analog currents. The analog I and Q currents are low-pass filtered by 3rd-order Butterworth g_m-C low-pass filters to attenuate the DAC spectral images before upconversion to RF. An RF loopback path from the output of the transmit RF mixer to the input of the receive RF mixer enables digital correction of RF impairments such as dc offset, I/Q mismatch, and RF carrier leak [3]. Shown in Fig. 20.2.5, are the 5GHz transmit phase noise and EVM for a 64QAM OFDM signal. The measured 5GHz and 2.4GHz EVM for 64QAM OFDM is -27.4dB and -27.5dB at an output power of -5.2dBm and -3.5dBm, respectively.

Low sleep and standby mode power dissipation is required in embedded WLAN applications in which the radio remains idle for a large fraction of the time. In sleep mode, the entire SoC is powered off until the host interface receives a wake-up command. Careful design of all analog blocks for low off-mode leakage current resulted in a sleep-mode power dissipation of <300µW of which ~180µW is from digital core leakage. In standby mode, the radio periodically toggles between an idle state in which only some analog bias and low-frequency digital circuits are active, and receive mode to listen for activity. Clock gating of inactive digital circuits, staggered power-up of analog blocks, and fast PLL and synthesizer settling reduce the standby mode power dissipation.

Fig. 20.2.6 shows a die micrograph of the dual-band WLAN SoC. The 6.64×6.72mm² die is packaged in a 2-layer 216-pin BGA package. The RF transceiver, data converters, baseband PLL, and analog pads occupy 13.5mm² of the die area. The measured performance of the radio, summarized in Fig. 20.2.7, successfully meets all the requirements of the IEEE 802.11a/b/g WLAN standard.

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References:
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[3] J. Thomson et al., "An Integrated 802.11a Baseband and MAC Processor," *ISSCC Dig. Tech. Papers*, pp. 126-127, Feb., 2002.

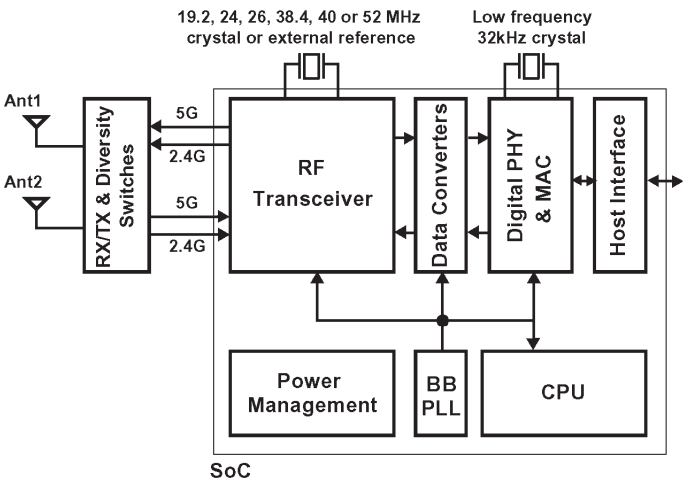

Figure 20.2.1: Block diagram of WLAN SoC.

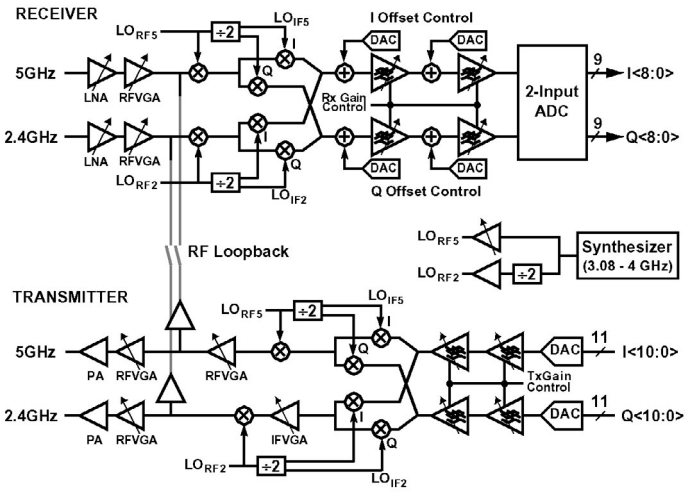

Figure 20.2.2: Dual-band RF transceiver architecture.

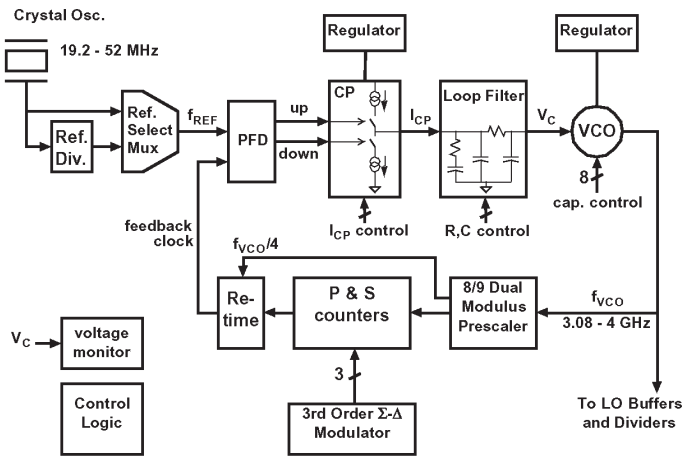

Figure 20.2.3: Fractional-N frequency synthesizer.

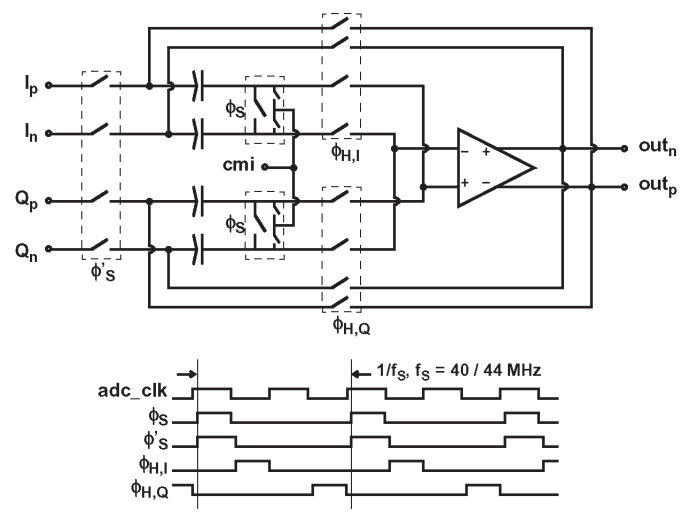

Figure 20.2.4: 2-input ADC Sample/Hold.

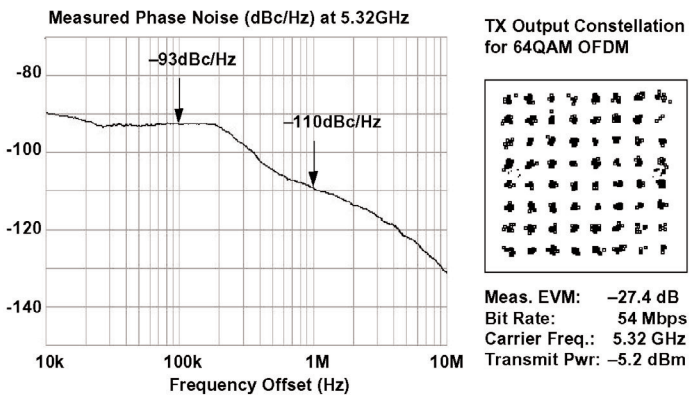

Figure 20.2.5: Measured 5GHz TX phase noise and EVM for 64-QAM OFDM.

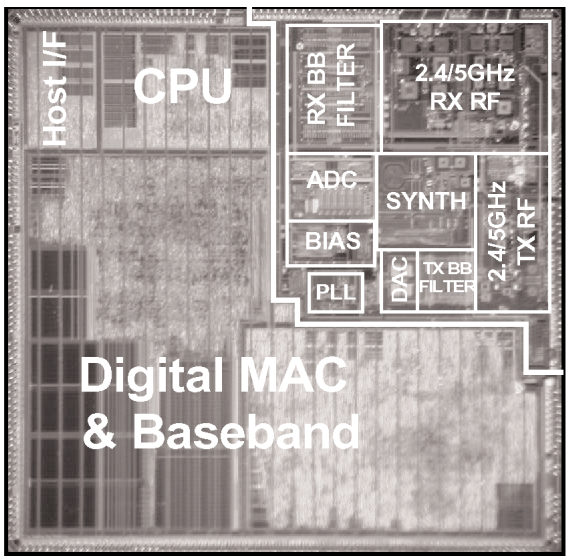

Figure 20.2.6: Chip Micrograph.

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Parameter	2.4GHz Band	5GHz Band
Transmit EVM at 54Mbps	-27.5dB @-3.5dBm	-28dB @-4dBm
Receiver Sensitivity at 6Mbps at 54Mbps	 -94dBm -76dBm	 -91dBm -73dBm
Receiver Noise Figure	5.0dB	5.5dB
Phase Noise @100kHz offset @1MHz offset	-99dBc/Hz -115dBc/Hz	-93dBc/Hz -110dBc/Hz
TX Mode Power Dissipation (@-4dBm) RF Transceiver (excl. DACs) complete SoC	@1.8V @3V 182mW + 90mW 290mW + 90mW	@1.8V @3V 220mW + 90mW 335mW + 90mW
RX Mode Power Dissipation RF Transceiver (excl. ADC) complete SoC	@1.8V @3V 158mW + 129mW 295mW + 129mW	@1.8V @3V 177mW + 90mW 308mW + 90mW
Sleep Mode Power Dissipation	< 300μW	
Technology	0.18μm 1P5M CMOS with 3V I/O	
Die Area RF Transceiver + data converters	44.6 sq. mm 13.5 sq. mm	
Package	2-layer, 216-pin BGA	

Figure 20.2.7: Performance summary.

